AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Canceled)

2. (Previously presented) The discrete time analog filter according to claim 16, further comprising means for direct sampling, wherein the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers.

3. (Currently amended) A discrete time analog filter comprising:

a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the single pole IIR filters are comprised solely of switches and capacitors; and

means for direct sampling, wherein the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers and ~~The discrete time analog filter according to claim 2,~~ wherein the means for direct sampling comprises a multi-tap direct sampling mixer.

4. (Previously presented) A high order filter comprising:

a cascade of single pole IIR filters configured to generate an output signal in response to an input signal;

means for direct sampling coupled to the cascade of single pole IIR filters;~~,~~ and

at least one amplifier stage coupled to the cascade of single pole IIR filters.

5. (Previously presented) A high order filter comprising:

a cascade of single pole IIR filters configured to generate an output signal in response to an input signal;

a multi-tap direct sampling mixer coupled to the cascade of single pole IIR filters; and

at least one amplifier stage coupled to the cascade of single pole IIR filters.

6. (Previously presented) The discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers

7. (Previously presented) The discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters is operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage.

8. (Previously presented) The discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters comprises a history capacitor coupled to a first rotating capacitor in a first capacitor bank.

9. (Previously presented) A discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input

signal, wherein the single pole IIR filters are comprised solely of switches and capacitors, a history capacitor being coupled to a first rotating capacitor in a first capacitor bank and a second capacitor bank comprising a buffer capacitor coupled to a second rotating capacitor, the second capacitor bank being coupled to the first capacitor bank.

10. (Previously presented) A discrete time analog filter comprising:

a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the single pole IIR filters are comprised solely of switches and capacitors;

a comparator responsive to the filter output signal to generate an output signal there from; and

a feedback loop coupling an output of the comparator to an input of the cascade of single pole IIR filters.

11. (Original) The discrete analog filter according to claim 10, wherein the cascade of single pole IIR filters together operate as a loop filter inside a sigma delta loop.

12. (Original) The discrete analog filter according to claim 10, wherein the input signal consists of an RF input signal minus a negative feedback signal flowing in the negative feedback loop.

13. (Original) The discrete analog filter according to claim 10, wherein the comparator comprises an ADC.

14. (Original) The discrete analog filter according to claim 13, wherein the ADC comprises a multi-bit flash ADC.

15. (Original) The discrete analog filter according to claim 10, wherein the negative feedback loop comprises a digital-to-analog converter (DAC).

16. (Previously presented) A discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the single pole IIR filters are comprised solely of switches and capacitors.

17. (Previously presented) A discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the cascade of single pole IIR filters comprises:

a history capacitor;

a first set of rotating capacitors, wherein at least one of the rotating capacitors is connected to the history capacitor;

a buffer capacitor connected to at least one of the rotating capacitors other than the at least one of the rotating capacitors connected to the history capacitor; and

a second set of rotating capacitors, wherein at least one of the second set of rotating capacitors is connected to the buffer capacitor.

18. (Previously presented) The discrete time analog filter according to claim 17, wherein after a predetermined period of time, at least one other of the rotating capacitors of the first set of rotating capacitors is connected to the history capacitor and at least one other of the rotating capacitors of the second set of rotating capacitors is

connected to the buffer capacitor, such that the respective rotating capacitors connected to the history capacitor and buffer capacitor operate in a ping-pong fashion.

19. (Original) The discrete time analog filter according to claim 17, wherein each set of rotating capacitors consists of two capacitors.

20. (Original) The discrete time analog filter according to claim 17, wherein the first and second set of rotating capacitors are configured as a pair of capacitor banks that operate in a ping-pong fashion with respect to one another.

21-23. (Canceled)

24. (Previously presented) A receiver front-end comprising:

a cascade of single pole IIR filters configured to generate an output signal in response to an input signal;

means for direct sampling coupled to the cascade of single pole IIR filters; and

at least one amplifier stage coupled to the cascade of single pole IIR filters, wherein the cascade of single pole IIR filters, the means for direct sampling, and the at least one amplifier stage together implement a high order filter.

25. (Previously presented) A receiver front-end comprising:

a cascade of single pole IIR filters configured to generate an output signal in response to an input signal;

a multi-tap direct sampling mixer coupled to the cascade of single pole IIR filters; and

at least one amplifier stage coupled to the cascade of single pole IIR filters, wherein the cascade of single pole IIR filters, the multi-tap direct sampling mixer, and the at least one amplifier stage together implement a high order filter.

26. (Previously presented) The receiver front-end according to claim 24, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers.

27. (Previously presented) A receiver front-end comprising:

a cascade of single pole IIR filters configured to generate an output signal in response to an input signal and being operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage;

means for direct sampling coupled to the cascade of single pole IIR filters; and

at least one amplifier stage coupled to the cascade of single pole IIR filters, wherein the cascade of single pole IIR filters, the means for direct sampling, and the at least one amplifier stage together implement a high order filter.

28. (Previously presented) A receiver front-end comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the cascade of single pole IIR filters comprises a history capacitor coupled to a first rotating capacitor in a first capacitor bank.

29. (Previously presented) A receiver front-end comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the cascade of single pole IIR filters comprises a history capacitor coupled to a first rotating capacitor in a first capacitor bank and a second capacitor bank comprising a buffer capacitor coupled to a second rotating capacitor, the second capacitor bank being coupled to the first capacitor bank.

30. (Previously presented) A receiver front-end comprising:

a cascade of single pole IIR filters configured to generate an output signal in response to an input signal;

a comparator responsive to the filter output signal to generate an output signal there from; and

a feedback loop coupling an output of the comparator to an input of the cascade of single pole IIR filters.

31. (Original) The receiver front-end according to claim 30, wherein the cascade of single pole IIR filters together operate as a loop filter inside a sigma delta loop.

32. (Original) The receiver front-end according to claim 30, wherein the input signal consists of an RF input signal minus a negative feedback signal flowing in the negative feedback loop.

33. (Original) The receiver front-end according to claim 30, wherein the comparator comprises an ADC.

34. (Original) The receiver front-end according to claim 33, wherein the ADC comprises a multi-bit flash ADC.

35. (Original) The receiver front-end according to claim 30, wherein the negative feedback loop comprises a digital-to-analog converter (DAC).

36. (Canceled)

37. (Previously presented) A receiver front end comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the cascade of single pole IIR filters comprises:

a history capacitor;

a first set of rotating capacitors, wherein at least one of the rotating capacitors is connected to the history capacitor;

a buffer capacitor connected to at least one of the rotating capacitors other than the at least one of the rotating capacitors connected to the history capacitor; and

a second set of rotating capacitors, wherein at least one of the second set of rotating capacitors is connected to the buffer capacitor.

38. (Previously presented) The receiver front-end according to claim 37, wherein after a predetermined period of time, at least one other of the rotating capacitors of the first set of rotating capacitors is connected to the history capacitor and at least one other of the rotating capacitors of the second set of rotating capacitors is connected to the buffer capacitor, such that the respective rotating capacitors connected to the history capacitor and buffer capacitor operate in a ping-pong fashion.

39. (Original) The discrete time analog filter according to claim 37, wherein each set of rotating capacitors consists of two capacitors.

40. (Original) The discrete time analog filter according to claim 37, wherein the first and second set of rotating capacitors are configured as a pair of capacitor banks that operate in a ping-pong fashion with respect to one another.